1. A method for making contact openings to devices on a substrate comprising the steps of:

forming a planar insulating layer on said substrate;

etching said contact openings of varying depths in said planar insulating layer to said substrate, while concurrently etching some of said contact openings extending over and along the edge of an embedded patterned conducting layer having an anti-reflective coating on its surface, embedded in said planar insulating layer, and thereby providing a means for forming contacts having low contact resistance to sidewalls of said embedded patterned conducting layer.

2. The method of claim 1, wherein said substrate is a semiconductor substrate.

3. The method of claim 1, wherein said devices include field effect transistors (FETs) comprised of gate electrodes and source/drain contact areas.

4. The method of claim 1, wherein said planar insulating layer having said embedded conducting layer is formed by:

forming a planar first insulating layer on said substrate;

etching node contact openings in said planar first insulating layer to said devices in memory regions and forming node contacts for capacitor bottom electrodes;

depositing and patterning a first conducting layer to form bottom electrodes over said node contacts;

forming sequentially a stacked layer whereby said stacked layer is formed by depositing an interelectrode dielectric layer, depositing a second conducting layer, which is said embedded conducting layer, and depositing said anti-reflective coating over said bottom electrodes, and patterning said stacked layer to form capacitor top electrodes, and thereby exposing sidewalls of said second conducting layer;

forming a planar second insulating layer on said substrate and over said top electrodes.

5. The method of claim 4, wherein said first and said second conducting layers are formed from materials selected from the group that includes polysilicon, titanium nitride, tantalum nitride, tungsten nitride, and ruthenium.

6. The method of claim 1, wherein said anti-reflective coating is a material selected from the group that

includes silicon oxynitride, titanium nitride, and tantalum nitride, and is formed to a thickness of between about 100 and 1000 Angstroms.

7. A method for making contact openings for a partially completed substrate having merged logic/dynamic random access memory (DRAM) comprising the steps of:

providing said substrate having devices in logic regions and memory regions, said devices surrounded and electrically isolated from each other by field oxide areas;

forming a planar first insulating layer on said substrate;

etching node contact openings in said planar first insulating layer to said devices in said memory regions and forming node contacts for capacitor bottom electrodes;

depositing and patterning a first conducting layer to form bottom electrodes over said node contacts;

depositing sequentially a stacked layer comprised of an interelectrode dielectric layer, a second conducting layer, and an anti-reflective coating over said bottom electrodes, and patterning to form capacitor top electrodes, and thereby exposing sidewalls of said second conducting lay r;

forming a planar second insulating layer on said substrate and over said top electrodes;

using a single masking step and etching said contact openings of varying depths in said second and first insulating layers for contacts to said devices on said substrate, and in said memory regions etching concurrently said contact openings extending over and along the edge of said top electrodes to expose said second conducting layer and providing a means for forming contacts having low contact resistance to sidewalls of said top electrodes.

8. The method of claim 7, wherein said substrate is a semiconductor substrate.

9. The method of claim 7, wherein said devices include FETs comprised of gate electrodes and source/drain contact areas.

10. The method of claim 7, wherein said planar first insulating layer is silicon oxide and is formed to a thickness of between about 3000 and 8000 Angstroms.

11. The method of claim 7, wherein said first conducting layer is polysilicon deposited to a thickness of between about 2000 and 15000 Angstroms.

12. The method of claim 7, wherein said interelectrode dielectric layer is silicon oxide/silicon nitride/ silicon oxide having a thickness of between about 20 and 150 Angstroms.

13. The method of claim 7, wherein said second conducting layer is a material selected from the group that includes polysilicon, titanium nitride, tantalum nitride, tungsten nitride, and ruthenium, and has a thickness of between about 50 and 3000 Angstroms.

14. The method of claim 7, wherein said anti-reflective coating is selected from the group that includes silicon oxynitride, titanium nitride, and tantalum nitride, and is deposited to a thickness that minimizes the optical reflectivity during photoresist exposure.

15. The method of claim 7, wherein said planar second insulating layer is silicon oxide and is formed to a thickness of between about 3000 and 20000 Angstroms.

16. A method for making contact openings on a substrate having merged logic/memory comprising the steps of:

providing said substrate having devices in logic regions and memory regions, said devices surrounded and electrically isolated from each other by trench isolation;

forming recesses in said trench isolation in said memory regions;

depositing and patterning a conformal first conducting layer and forming capacitor bottom electrodes in said recesses;

depositing sequentially a stacked layer comprised of an interelectrode dielectric layer, a second conducting layer, and an anti-reflective coating over said bottom electrodes;

patterning said stacked layer to form capacitor top electrodes, and concurrently forming open areas in said top electrodes to said trench isolation, and thereby exposing sidewalls of said second conducting layer;

forming a planar insulating layer on said substrate and over said top electrodes;

using a single masking step to etch said contact openings of varying depths in said insulating layer for contacts to said devices on said substrate, and in said memory regions, etching said contact openings extending over and along the edge of said top electrodes in said

open areas to expose said second conducting layer and providing a means for forming contacts having low contact resistance to sidewalls of said top electrodes.

17. The method of claim 16, wherein said shallow trench isolation has a thickness of between about 2000 and 6000 Angstroms.

18. The method of claim 16, wherein said shallow trench isolation is recessed to a depth of between about 500 and 4000 Angstroms.

19. The method of claim 16, wherein said conformal first conducting layer is polysilicon.

20. The method of claim 16, wherein said anti-reflective coating is selected from the group that includes silicon oxynitride, titanium nitride, and tantalum nitride, and is deposited to a thickness that minimizes the optical reflectivity during photoresist exposure.

21. The method of claim 16, wherein said planar insulating layer is silicon oxide and is formed to a thickness of between about 3000 and 8000 Angstroms.

22. The method of claim 16, wherein at least two of said contact openings are etched over said edge of said top electrodes in said open areas on opposite sides of said open areas to allow for more relaxed alignment tolerances.

23. The method of claim 16, wherein a multiple of said contact openings are etched in series that is skewed to said edge of said top electrodes on opposite sides of said open areas to allow for more relaxed alignment tolerances.

24. The method of claim 16, wherein a multiple of said contact openings are etched in series along said edge of said top electrodes in said open areas, and wherein said contact openings are elongated normal to said edge of said top electrodes in said open areas to allow for more relaxed alignment tolerances.

25. A planar insulating layer with contact openings on a substrate having device areas comprised of:

a conducting layer having an anti-reflective coating on top surface and patterned to have open areas on said substrate;

said planar insulating layer on said patterned conducting layer having said contact openings of

varying depths to said device areas, said contact openings formed using a single masking and etching step;

some of said contact openings extending down to and over edge of said patterned conducting layer within said open areas for forming low-resistance contacts to said edge of said patterned conducting layer.

26. The structure of claim 25, wherein at least two of said contact openings are etched over said edge of patterned conducting layer in said open areas on opposite sides of said open areas to allow for more relaxed alignment tolerances.

27. The structure of claim 25, wherein a multiple of said contact openings are formed in series that is skewed to said edge of said patterned conducting layer on opposite sides of said open areas to allow for more relaxed alignment tolerances.

28 The structure of claim 25, wherein a multiple of said contact openings are etched in series along said edge of said patterned conducting layer in said open areas, and wherein said contact openings are elongated

normal to said edge of said patterned conducting layer in said open areas to allow for more relaxed alignment tolerances.

29. The structure of claim 25, wherein said patterned conducting layer is the top electrode of a capacitor.

30. The structure of claim 25, wherein said anti-reflective coating is a material selected from the group that includes silicon oxynitride, titanium nitride, and tantalum nitride, and is deposited to a thickness that minimizes the optical reflectivity during photoresist exposure.